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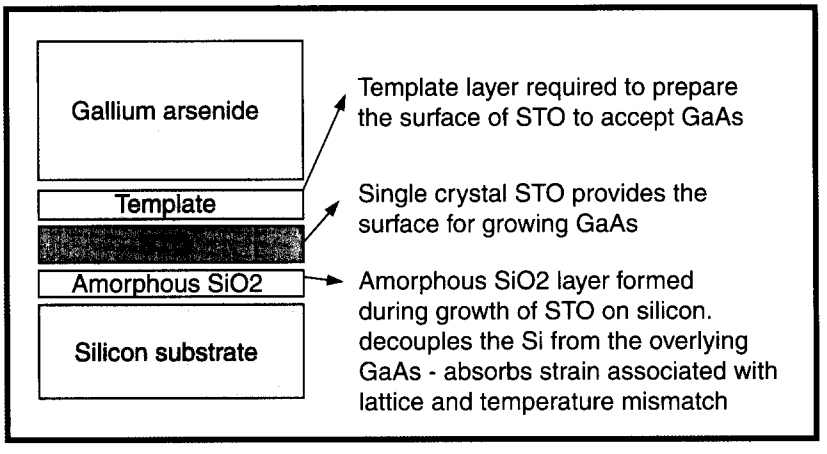
For more than 20 years many millions of dollars have been spent for the growth of gallium arsenide and other hetero-materials on silicon for all the obvious reasons, larger, cheaper and higher quality substrates available in quantity (mostly elemental Groups III-V and II-VI). Unfortunately most of it was spent producing either little success or a cost in excess of the competing compound semiconductor substrate. And, for some time the only compound semiconductor that showed promise was silicon-germanium, which does not quite present the same technology challenge, since both elements are in the same Group IV of the Periodic Table and therefore the silicon-germanium material system may be classed as an alloy rather than a compound.

Compound Semiconductors on Silicon

The results of combining these dissimilar materials are now in from several research groups and they are close to changing the outlook for these inter group, or hetero-epitaxial processes from dim to very promising or even to almost commercial, (based on the latest gallium arsenide and gallium nitride on silicon process advances). As reported in III-Vs Review earlier this year, Motorola and IQE have been cooperating to develop the deposition of MBE-grown gallium arsenide on silicon wafers for about one year. This cooperation between Motorola and IQE already includes a Custom Evaluation Agreement open to IQE and Motorola customers, a Service and Cooperation Agreement in which Motorola will purchase development services from IQE, a $10 million equity investment by Motorola in IQE, a $14 million three year equity draw down facility for IQE and an additional $10 million purchase of warrant options in IQE, extending over five years.

2000Å of a gallium arsenide seed layer are deposited to form a pseudo substrate



Gallium Arsenide

The Motorola process involves the use of high dielectric-constant oxide-interlayers, such as strontium titanate (STO), which inhibit reaction between the silicon and the epitaxially grown gallium arsenide layers. If electrical conductivity to the substrates is required, the STO layer can be doped with concentrations of up to 10E19 atoms per cm^3 of aluminium. The crystalline quality of this STO on silicon is reported to be better than any single crystal STO currently available. Originally, Motorola's interest in this technology was the creation of a compliant substrate for the deposition of epitaxial, high dielectric constant oxide films on silicon for random access memory devices, a concept previously proposed in 1991 by Cornell Professor, Y.H. Lo.

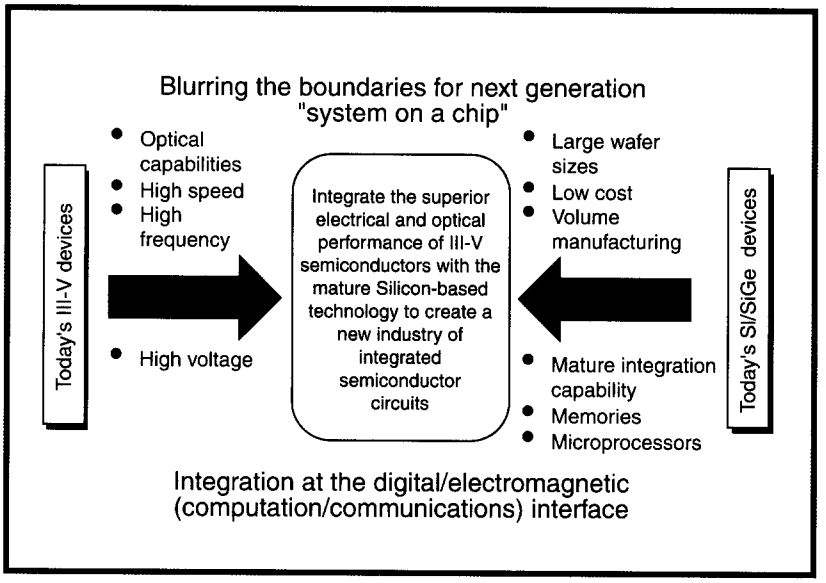
One of the keys to this type of hetero-epitaxy and one of the processes developed by Motorola, is the formation during growth of a thin silicon dioxide interlayer between the surface layer of

silicon and the mechanical support silicon wafer however, the 20Å silicon dioxide layer originally produced in the process was unsuitable for CMOS applications and has been replaced by an STO layer. This thin oxide can be either amorphous or crystalline, but it serves to take the stress out of the surface silicon layer and allows the growth of a low stress hetero-epitaxial layer on the surface. In the case of strontium titanate interlayers, the optimised STO layers are about120 Å thick, with the silicon dioxide interlayer thickness reduced to 7 angstroms.

Following the deposition of the STO layer, at least 2000Å of a gallium arsenide seed layer are deposited to form the pseudo substrate, suitable for gallium arsenide device layer growth and possibly other III-V materials on silicon. Rather fortuitously, a thin silicon dioxide layer, which is compliant and forms between the silicon and the STO layer. The STO has a stable cubic structure above 70° Kelvin and it allows the stresses, the thermal interlayer mismatches and the associated cracking to be eliminated. It also creates the possibility for lattice engineering, which could be the enabler for new device structures. Currently, only solid sources are used in this MBE deposition process, requiring high temperature Knudsen Cells to produce the vapourised metals and good control of the gas injection, creating a challenge for solid source MBE technology.

For process development, IQE used a Gen-2000 MBE reactor with a 7 x 6" wafer capacity and separate III-V and oxide deposition chambers where the oxide inter-layer and the seed gallium arsenide layer are grown separately. Various silicon substrate resistivities have been used and 1 to10 ohm-cm material can make good RF devices. However, the higher resistivity (1000 to 5000 ohm-cm) float zone silicon substrates may be preferable for high frequency devices, but they have not yet been evaluated. Process uniformities are good with the deposited STO layer thicknesses and GaAs MESFET across the wafer resistivities exhibiting better than 1% uniformities.

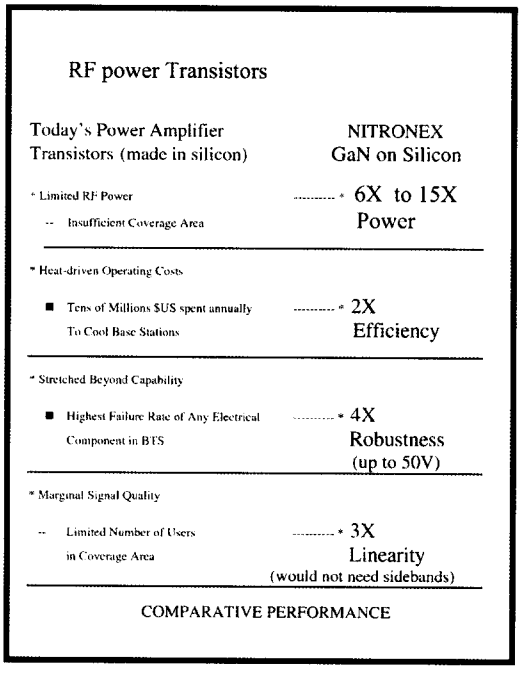
To realize its low cost potential, a high volume process and product is needed that could provide additional customer feed back. The key factors to support a manufacturable process are stated to be minimal operator involvement, full process computerization, accurate control of material beams and process parameters and a need to keep device re-engineering for existing



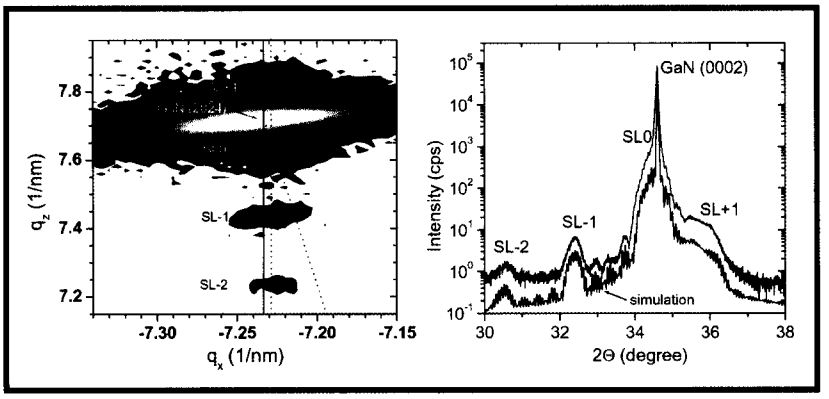
The best of both worlds

products to a minimum. According to Thomas Hierl, the CTO of IQE plc, the process is production capable, but development volumes are needed to corroborate the initial data for reproducibility, yields and costs. With suitable demand, scale up to production volumes would be possible by Q1 2003.

With deposition uniformities already similar to those attained from gallium arsenide on gallium arsenide processes (homo-epitaxy), a ramp up to commercial volumes could be accomplished within one year. The target price for the 6" gallium arsenide on silicon wafers is $200 for 6" diameter pseudo substrates versus a reported price of $300 for 6" gallium arsenide wafers although pseudo-wafer costs in the development phase are believed to be in the $400 to $600



nitride power transistors and amplifiers can easily outperform silicon



Reciprocal-space map around the GaN (20$\bar{2}$4) reflection (left) and Θ-2Θ scan (right) showing measurement and simulation. As can be clearly seen in the reciprocal space map the superlattice (SL) peaks are slightly shifted in q_x with respect to the main GaN reflection indicating a different a-lattice constant (vertical dashed line) but no relaxation (partial relaxation: diagonal dashed line). The Θ-2Θ scan shows, in addition to the superlattice peaks, Pendellösungs fringes from the SL and the cap layer, indicating the high quality of the InGaN/GaN interfaces.

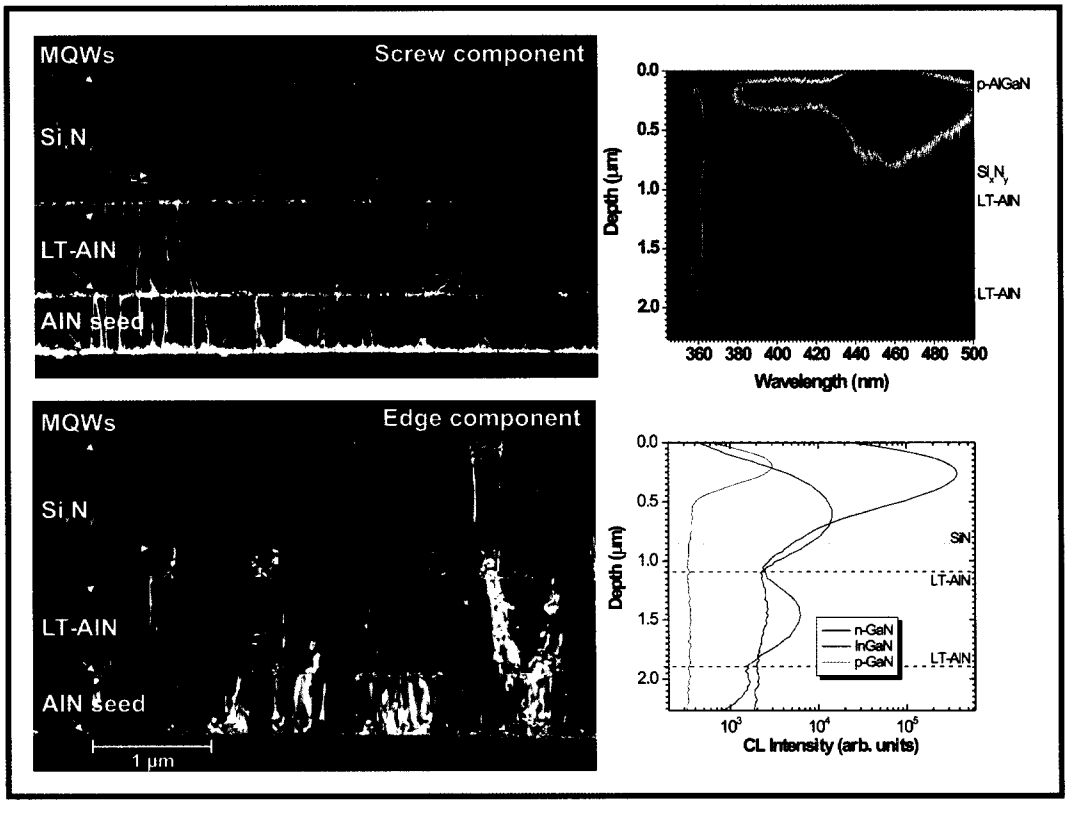
range. FETs have already been demonstrated based on this process and it is now being extended to heterobipolar-devices. To promote high interest levels and participation in their gallium arsenide on silicon technology and to reduce development costs for interested parties, Motorola has agreed to allow interested companies to proceed with process development work without a license by using non-disclosure agreements.

To speed up the progress of the gallium arsenide on silicon technology internally, Motorola has formed a wholly owned subsidiary, Thoughtbeam Inc., headed by Padmasree Warrior as General Manager. Although Thoughtbeam is an R&D operation without a fab, its goal is to combine the best of the III-V and the silicon worlds. Using the MBE grown pseudo substrates and depositing the active device layers by MOCVD, Motorola has already compared the performance of their gallium arsenide on silicon FETs with similar gallium arsenide based devices and shown them to have similar characteristics including, mobilities, saturated velocities, gate/drain breakdown voltages, transconductances and RF performance. MESFET power amplifiers based on this technology with equivalent power efficiencies have already been evaluated in cellphone handsets in the Chicago area and were found to be indistinguishable from those on gallium arsenide wafers. Future plans include the testing of HBTs and lasers.

Gallium Nitride

The potential for gallium nitride devices covers a wide range of application areas and includes those listed below.

- Power conditioning
- Wireless broadband
- Pressure sensing
- White solid-state lighting



Weak-beam TEM images using (0001) and (1$\bar{1}$00) reflection to view screw type (top left) and edge type (bottom left) dislocations, respectively. In the TEM image the reduction of dislocation density due to the LT-AlN interlayers (C) and the Si_xN_y in-situ mask (B) can be clearly seen. A denotes the AlGaN:Mg/5x(InGaN/GaN:Si) active region and D the AlN seed layer. CL linescans taken at 5 K for the same cross section are plotted on the right side on the same scale. On the top-right, a spectrum linescan is plotted depicting the vertical evolution through the layer sandwich. On the bottom-right, intensity profiles are plotted for the n-GaN, p-GaN and InGaN luminescence, respectively.

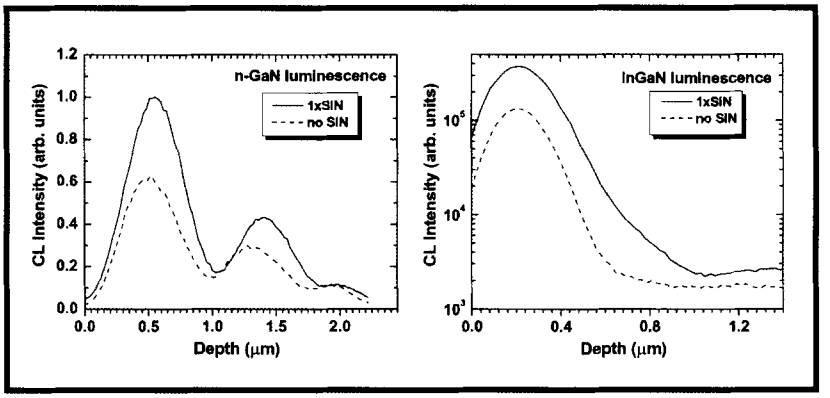
- DVD storage
- Coloured signs & lighting
- Automotive lighting
- Automotive electronics
- Power transmission
- Heat sensing
- Flame sensing
- Telecomm base stations
- Satellite electronics

LED lighting products are well established and are a high grow rate applications category, with blue and violet lasers being aggressively developed for high capacity DVDs, but the potential for electronic devices is yet to be realized. Two key factors have contributed to the slow introduction of nitride devices and they are the high defect levels inherent in most epitaxial nitride layers and the lack of bulk substrates for homo epitaxy. These necessitate the use of hetero-substrates, such as sapphire and silicon carbide.

In many instances, military need and performance have driven the development of new compound semiconductor materials, processes and devices but cost has driven process development for the higher volume products (as in silicon devices). However, a company called Nitronex plans to simultaneously combine the advanced hetero-substrate growth technologies and the anticipated lower cost features inherent in gallium nitride on silicon in their SIGANTIC process, to create a 'revolutionary potential' for their nitride on silicon technology, with an initial goal of $60 for a 60W chip.

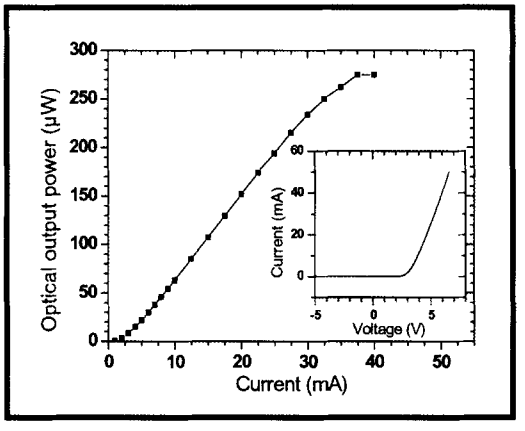
Nitronex has licensed North Carolina State University patents covering the deposition of gallium nitride on silicon, a process they are developing for the commercial production of both electronic and optoelectronic gallium nitride devices. Originally, the focus was reported to be the use of a pendeo-epitaxy processes, but after reviewing the key patents, the adoption of a silicon carbide interlayer process (between the silicon and the gallium nitride layer) seems to be more appropriate than the incorporation of pendeo technology.

In the Nitronex processes, an upper silicon layer (with a preferred 111 orientation), [selected from either a bulk silicon, a silicon on insulator (SOI) or a silicon over implanted oxygen (SIMOX) wafer substrate] is converted at a high temperature into a 3C-silicon carbide layer by treatment with a carbon containing precursor gas such as ethylene. As an alternative, silicon carbide can also be directly deposited on the silicon wafers. If not, the carbide seed layer may then be thickened by the further chemical vapour deposition growth of additional silicon carbide. After a polishing step to smooth out the deposited silicon carbide, a thin, low temperature buffer layer (in the range of 50 to100nm thick) of either aluminium or gallium nitride is usually grown. It is on this buffer layer that the device layers of 2H-gallium nitride and its alloys are usually deposited with the best defect levels achieved being in the 10E6 per cm² range. The use of substrates with the oxide interlayers may also provide the added benefit of a compliant substrate, where stress relief is obtained by slippage between the silicon and its adjacent oxide layer.



CL linescans from the top of the diode structure to the substrate of the two LED samples, with and without a Si_xN_y interlayer, showing the n-GaN (left) and InGaN luminescence (right). A strong enhancement in CL intensity is observed for the n-GaN luminescence after each LT-AlN interlayer, which are located at the two minima around 1 and 1.7 μm. A strong enhancement of the InGaN luminescence by the Si_xN_y interlayer is also observed. This is due to a better InGaN quality and a better carrier diffusion clearly indicated by the prolonged tail of the InGaN luminescence for the sample with SixNy mask.

Masking layers or trenches can be added prior to the last growth step in which case, device quality lateral epitaxial over growth (LEO) or pendeo-epitaxial layers of 2H-gallium nitride can be produced. Such layers may have lower defect levels over the masked areas than those obtained by direct growth on the seed layers. Additionally, it is envisaged that sections of the silicon wafer may be capped off so that they are not converted to carbide or gallium nitride layers. After removal of the cap, they could then be used to grow silicon devices (or even expose silicon devices already

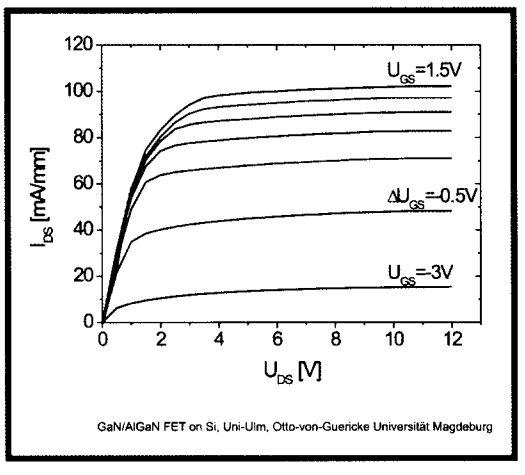


I-V characteristics of a vertically contacted light emitting diode grown on Si substrate (inset) and power vs. current of an LED (360 μm diameter) mounted on an ~ 1 mm² die in an epoxy LED dome. At 35 mA Ohmic heating starts to significantly reduce device performance. The peak wavelength is around 455 nm.

prepared), creating the potential for both silicon and gallium nitride devices on the same chip.

According to John Brewer, Jr. Vice President, Marketing at Nitronex, their first gallium nitride product target is the telecommunications base station, where nitride power transistors and amplifiers (with the capabilities for higher power levels, higher efficiencies [40 to 60%], higher operating voltages and the ability to operate at higher junction temperatures) can easily out perform the silicon LDMOS presently in use. This is quite a large market where the number of transmit/receive circuit boards are expected to increase from about 7 million last year to over 15 million in 2004 and their corresponding value to increase from almost $600 million to $1.25 billion in the same period. This value represents over 25 million power amplifiers. Only the lack of reliability data and perhaps design acceptance should stand in their way. To meet these goals, the Nitronex strategy is for cross-industry partnerships rather than a control of the market, and therefore the Company has cooperative process development agreements available for partners interested in these and other nitride-on-silicon based applications.

There are several reasons for this opportunity, first the silicon circuits are not very power efficient (more than 80% of the power is dissipated as heat), second, a high air conditioning cost in the region of $10 million per system for removing this heat and third, a relatively short operating lifetime (6 to 9 months) for the silicon power amplifiers due to their high junction operating temperatures. Another incentive for the adoption of gallium nitride amplifiers is their superior linearity, which would allow closer spacing of user channels, less side band allocation and more users per existing base station. The system demands from third generation mobile handsets could drive the insertion of gallium nitride devices in the 2003/2004 time frame for reasons of efficiency, linearity and higher operating voltages.

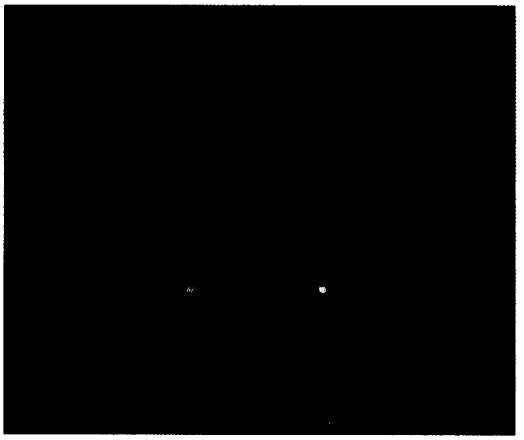


FET performances, with ft of 11GHz and fmax of 17GHz were not as good as expected

As reported in the previous issue of III-Vs Review, (Vol. 15 page 40), a University of Magdeburg research group around Alois Krost is also developing gallium nitride on silicon device processes and presented its results on the development of their III-nitride-on-silicon process at the recent Materials Research Society Meeting in Boston. The Magdeburg processes use either masking or superlattice inter-layers to prepare the silicon for acceptable nitride growth. Process development has evolved to where gallium nitride blue LEDs have already been demonstrated on nitride layers deposited on silicon wafers grown by the NCSU and the Magdeburg developed processes.

Additional progress has been made and in a private communication, Armin Dadgar from the University of Magdeburg reported on a cooperative effort with Global Light Indistries (GLI) in Germany, where Markus Kamp et al manufactered blue and green LEDs employing buffer structures prepared in Magdeburg. The active LED structure has been grown by Andreas Kaluza's MOCVD group using planetary reactors. Processing and packing used standard GLI processes. See the photograph of these packaged nitride on silicon LEDs operating at a 20mA drive current. I-V characteristics of the front contacted diodes were as good as those GaN/sapphire LEDs, giving operation voltages around 3.1V at 20mA current.

Even though the I-V characteristics for front-contacted LEDs on silicon and sapphire were identical, the output power of the planetary-grown LEDs on silicon was lower (approximately 0.2mW at 490nm and 0.4mW at 498nm) than for those grown on sapphire. However, neither epitaxial growth nor processing has been adjusted to the different substrate. Further improvements in output power are expected from the removal of the absorbing Si substrate. It is worthy of note that the in situ insertion of a silicon nitride mask (which has been used to lower the defect densities on sapphire and silicon) significantly increased the optical output power and that all the LEDs grown on silicon are red-shifted by 20 to 40nm, when compared with LEDs grown on sapphire. This factor makes a direct comparison of the diodes difficult. The shift is presumed to



Global Light Industries LEDs

be due to the presence of tensile stress on silicon versus compressive stress on sapphire.

Transmission electron microscopy analyses on cross sections of these LED structures have now been performed by O. Contreras and F.A. Ponce from Arizona State University. The dual aluminium nitride inter layers and other structural layers in this gallium nitride on silicon system are clearly visible, together with the differing levels of defects created as the structure was being grown. Note also the cathode luminescence line scan intensity data and a layer map for the same structural cross sections. These were determined by T. Riemann and J. Christen from Magdeburg. An increase in luminescence intensity is obtained after each aluminium nitride layer is inserted.

In cooperative research with the University of Ulm and extending the process to electronic devices, the first gallium nitride FETs on silicon have now been made. The undoped AlGaN/GaN FET devices exhibited good two-dimensional electron gas results with mobilities of 1590 cm^2/Vs at reasonably high carrier concentrations (6.7E12 per cm^2). The FET performances, with ft of 11GHz and fmax of 17GHz were not as good as expected and were attributed to sub-layer parasitic currents. Future modifications of the growth process are planned and should improve the performance of these FETs.

The growth of compound semiconductors on silicon is now a revisited topic of interest and in some instances believed to be in the almost commercial category. At the recent Gorham conference, Compound Semiconductor Outlook 2002, the growth of compound materials on silicon was offered as a one-day tutorial session. For those interested in either gallium arsenide or gallium nitride on silicon process technology, the tutorial was a worthwhile feature and a relatively painless way to catch up with the wave. The potential market for these processes was well documented and many opportunities were explored, but little information was offered about the current process costs, except for the 3x estimate for gallium arsenide pseudo wafers reported by Thomas Hierl from IQE (at their present state of development). Volume production is expected to bring these pseudo substrates into competition with those available today. When successful, growth on silicon could offer an agility to switch from one materials business model to another. Additionally, there may be an incentive for the telecommunications providors to support these and other compound solutions for bandwidth expansion, since voice provides most of their income, but data is now the largest consumer of the available bandwidth capacity.